# Teraflop (10E15) Supercomputing

# Design Note #18

10E15 Teraflop Computer Performance requires exacting design techniques

Compaq Computer Corporation, a world wide provider of supercomputer hardware systems, engaged Orchid Technologies to perform the electronic hardware and test firmware design of its new Wildfire Teraflop Computer's IO System.

## Raw Computing Performance

A single Wildfire IO Shelf is capable of supporting up to eight simultaneous 64 bit wide PCI Buses. Each PCI bus may be fully loaded thereby producing an IO Subsystem of unmatched throughput. Achieving this level of performance requires calculated, specialized electronic circuit board design techniques.

## ECL Signal Quality Matters

Multiple, high-speed ECL clock signals are distributed throughout the unit with sub-nano second maximum skew requirements. Full differential ECL signaling require specialized power system design, signal termination, and signal pair routing needs.

## High Speed Design Matters

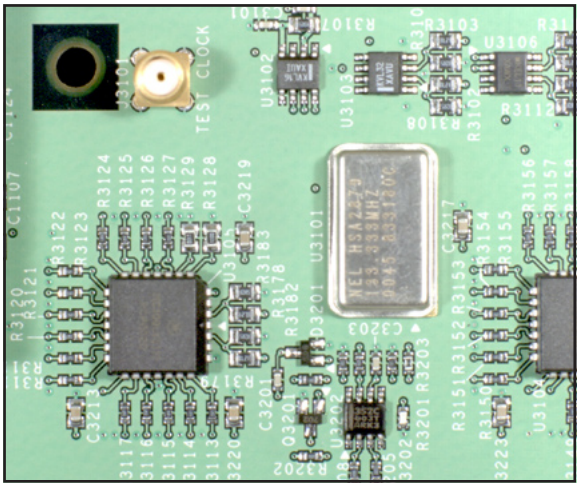
With on-board base clock rates to 133MHz, controlled impedance, controlled differential pair routing, controlled cross-talk, and controlled signals, lengths matter. At these on-board signal rates, each circuit is its own work of art. Each circuit requires rigorous attention to detail.

## Power System Noise Matters

Circuit board infrastructure is as important to successful high speed design as the high-speed signals themselves. Carefully controlled ECL voltage planes, proper attention to high-speed phase lock loop circuits and proper grounding techniques all contribute to the successful high speed system.

## When Details Matter

Orchid Technologies has performed numerous, challenging high-speed system designs. From 33MHz to 300MHz, Orchid understands what it takes to produce a properly terminated, low-signal reflection balanced system. Call Orchid today. Let us design a high performance system for you too.

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**Custom Engineering From Concept to Production**

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